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A Full Subtractor Design with Improved Performance

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ABSTRACT: Full subtractors are used in various numerical applications. A full subtrractor for two n bit numbers has three inputs namely two n-bit inputs and one borrow in from previous pair of bits for each n bits and two outputs namely n-bit. difference and one final borrow. The total number of ports is 3n+1.This paper proposes n-bit full subtractor design by considering the values of inputs eliminating the borrow in inputs for calculation of result. The total number of ports is 2n+1. Expressions for difference and borrow are derived from the various cases. The proposed design is simulated in Quartus2 toolkit using verilog code for eight bit inputs. An reduction in number of pins by 24.24% with performance improvement of 10.35% comparable number of logic elements and comparable power dissipation is observed for the chosen parameters

KEYWORDS: area, full.Subtractor, power consumption, timing

I.INTRODUCTION

The CPU of computer has arithmetic logic unit ALU and control unit CU. The ALU has circuits for arithmetic operations and logic functions. Add,subtract,multiply and divide are common arithmetic operations. Many algorithms for these operations are proposed in literature.A. Full subtractor performs subtraction of subtrahend from minuend . It has three inputs and two outputs. The inputs are minueend, subtrahend, borrow in. The two outputs are difference and borrow out. The truth table of full subtractor is given in Table1

Table1 Full subtractor truth table

Minu end	Subtra hend	Borr ow in	Diffe rence	Borro w out
B0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

From Table1 the expressions for difference and borrowout for any inputs a,b,bin, outputs diff,bout is given below
Difference =a XOR b XOR bin (1)
Bout =!a&bin OR !a&b OR. b&bin (2)
There are two XOR gates to calculate difference,three AND and two OR gates to calculate borrow out.

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The authors in [1] gives the common way to perform subtraction using two's complement. The disadvantage with full subtractor is to express negative numbers when subtrahend is greater than minuend. Two's complement scerts this case. The authors in [2] compare various methods to implement full subtractor. They concluded that XOR based full subtractor gives better performance and GDI base full subtractor gives power savings. The authors in [4] compare three designs of full subtractor with XOR gates and 2to1 MUX and suggest the best design.

The authors in [3] compare for powe dissipation and temperature full subtractor design in various FPGA families.
This paper proposes algorithm to calculate difference of two inputs. The proposed algorithm considers the bit pattern of input b and borrow in to assign difference and borrow out input literal. The borrow out at stage-i of n-bit input pair is borrow in of stage i-1. The algorithm reduces number of gates in computations. The algorithm requires only two inputs to calculate difference. The proposed model is simulated for 8 bit inputs in Quartus 2 toolkit. A reduction in number of pins by 24.24% with performance improvement of 10.35% comparable number of logic elements and comparable power dissipation is observed for the chosen parameters .

This paper is organised as follows. Section 2 is motivation, section 3 is proposed model, by section 4 is simulation, section 5 is conclusion followed by references.

II. MOTIVATION

Example1
Consider 1100-1010. The minuend is a[3:0]=1100 and subtrahend b[3:0]=1010.

The Table2 gives the calculation using full subtractor truth table Table1

Table2. Calculate 1100-1010

I	a[I]	b[I]	Difference	Borrow
0	0	0	0	0
1	0	1	1	1
2	1	0	0	0
3	1	1	0	0

As seen from Table2 the result is 0010 with final borrow zero. Next consider following algorithm. Let borrow[0:3] be 4 element array initialised to 0. For any pair of inputs bits a,b and borrow bin=0
1. Start
2. if b=bin then
Duff =a
Bout =b
Go to step 4
3. if b <> bin then
Duff= not a
Bout = not a
4. stop
Duff is the difference and Bout is borrow out.
The above steps applied to Example1 gives the following.

Table 3 proposed algorithm example

I	A[I]	B[I]	Borrowin	Difference	Bout
0	0	0	0	0	0

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1	0	1	0	1	1
2	1	0	1	0	0
3	1	1	0	0	0

As seen from Table3 difference =0010 and borrow =0. The number of XOR gates is reduced in the calculation of difference from eight to zero for given example of four bits. The difference is assigned a literal. Hence four literals are required. The borrow in at bit-i requires three AND and two OR gates is reduced to one literal. There is decrease in number of inputs reduced by borrow in of four bits. This is the motivation of this paper.

III.PROPOSED ALGORITHM

Consider full subtractor. It has three inputs a,b, bin and two outputs duff, bout. The truth table is given in table1. From Table1 the expressions for diffence and borrow out are given below
Difference =a xor b xor bin
Borrow = bout =(!a and bin)or(!a and b) or (b and bin)

Consider the following cases
Of the inputs.
1 if b=bin then
Duff =a
Bout =b
Go to step 3
2 if b <> bin then
Duff= not a
Bout = not a
3 stop
In above, Duff is difference Bout is borrow out.
The number of gates in difference is reduced to one in worst case and in borrow out is reduced to one gate.
This is opposed to traditional equations as given in (1),(2) where difference has 3 xor gates and borrow out is 3 and gates and two or gates

IV.SIMULATIONS

The proposed algorithm in section 3 is simulated using Quartus2 toolkit and verilog code. The proposed model is compared with traditional full subtractor model.
The simulation parameters are shown in Table3.

Table4 simulation parameters

Parameter	Value
Processor	Cyclone2
Package	FBGA
Pins	484
Speed	Fastest
Clock frequency	5MHz

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The proposed model is called prop in this paper. The traditional full subtractor is used for benchmark. This model is called trad in this paper. The simulation results are shown in Table4.

Table 5 simulation results

Parameter	Trad	Prop	%improcement
Timing(ns)	16.198	14.522	10.35
#pins	33	25	24.24
#logic elements	17	18	-0.06
Power (mW)	70.58	69.65	1.32

As seen from Table3 performance improvement of 10.35% with 24.24% reduction in pins with comparable number of logic elements along with comparable power consumed. for proposed model compared with traditional model.

V.CONCLUSION

A full subtractor design is proposed in this paper. The proposed model eliminates the borrow in input in calculation of difference, borrow out. It compares values of borrow in with one of inputs b and decides difference and borrow out for any pair of inputs. The borrow in in bit-i is the borrow out at bit i-1. The proposed model is simulated with Quartus2 toolkit. A performance improvement of 10.35% with 24.24% reduction in pins ,comparable number of logic elements along with comparable power consumed is observed in proposed model compared with. traditional model.

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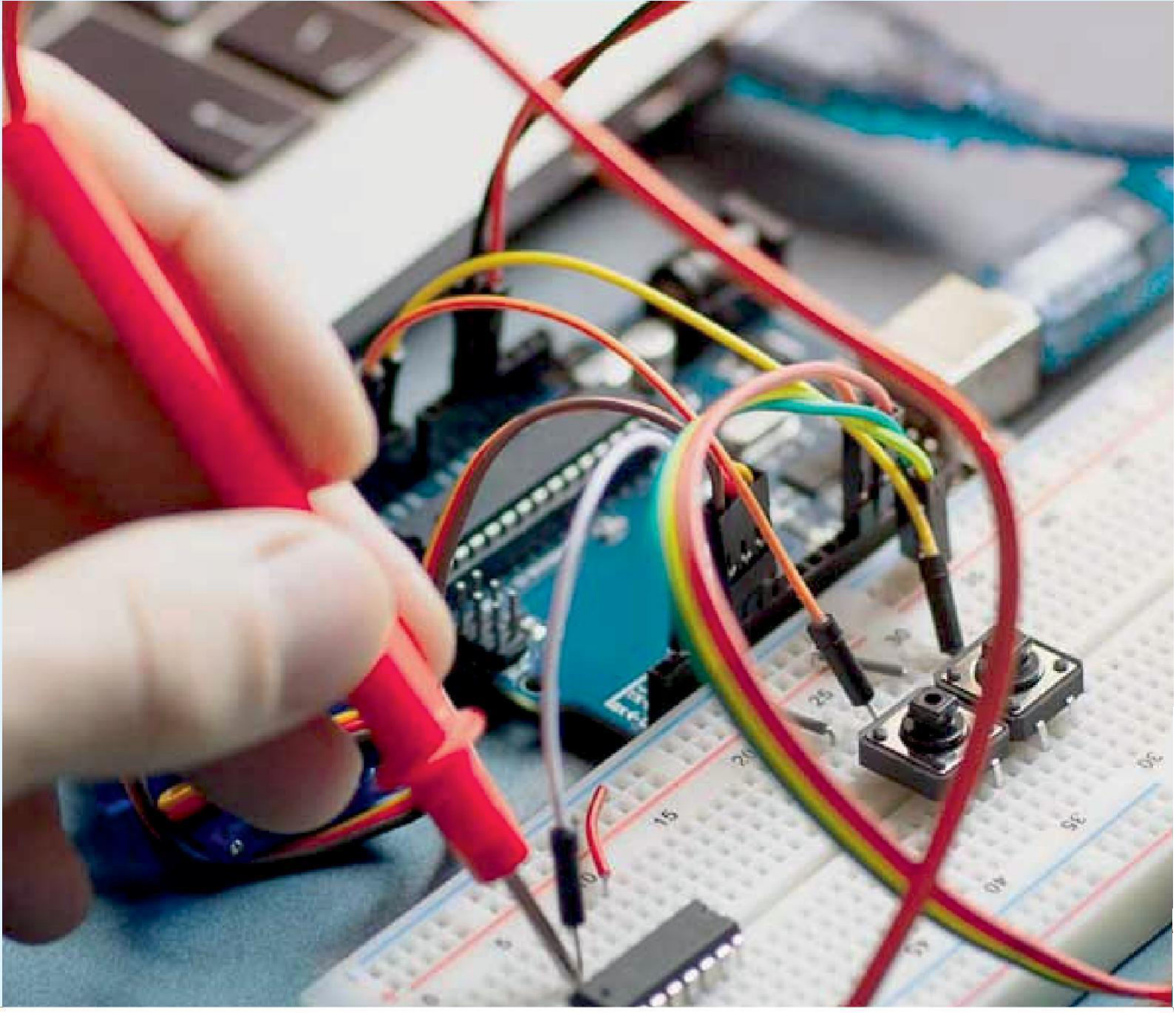

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